1. A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images in portions of said photoresist layer lying in said selected fields overlying said test pattern of said first layer; and

d) measuring the alignment of said test pattern in said selected fields of said first layer with said overlying latent images in said photoresist layer using scatterometry.

2. The process of claim 1 wherein said test pattern formed in said selected fields of said first layer comprises a test pattern of lines.

3. The process of claim 2 wherein said test pattern of lines formed in said selected fields of said first layer comprises a test pattern of parallel spaced apart lines.

4. The process of claim 2 wherein said test pattern of lines formed in said selected fields of said first layer comprises a test pattern of parallel spaced apart metal lines.

5. The process of claim 3 wherein said latent images formed in said portions of said photoresist layer lying in said selected fields overlying said test pattern of lines comprises a pattern of parallel spaced apart lines.

6. The process of claim 5 wherein said latent images of parallel spaced apart lines, formed in said portions of said photoresist layer lying in said selected fields overlying said test pattern of parallel spaced apart lines formed in said selected fields of said first layer, are formed generally parallel to said test pattern of parallel spaced apart lines formed in said selected fields of said first layer, whereby said test pattern of parallel spaced apart lines formed in said selected fields of said first layer and said latent images of parallel spaced apart lines formed in said portions of said photoresist layer lying in said selected fields form a diffraction grating, the accuracy of which is measured by said scatterometry to determine the alignment of said layers of lines.

7. The process of claim 6 wherein said latent images of parallel spaced apart lines are interspaced between said test pattern of parallel spaced apart lines formed in said selected fields of said first layer.

8. A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern of parallel spaced apart lines in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images of parallel spaced apart lines in portions of said photoresist layer lying in said selected fields overlying said test pattern of parallel lines of said first layer, said parallel lines of said test pattern of said first layer generally parallel with said parallel lines of latent images in said photoresist layer; and

d) measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry.

9. The process of claim 8 wherein said test pattern of parallel spaced apart lines formed in said selected fields of said first layer comprises a test pattern of parallel spaced apart metal lines.

10. The process of claim 8 wherein said latent images of parallel spaced apart lines formed in said photoresist layer and said test pattern of parallel spaced apart lines formed in said first layer are formed generally parallel to one another to form a diffraction grating, the accuracy of which is measured by said scatterometry to determine the alignment of said layers of lines.

11. The process of claim 10 wherein said latent images of parallel spaced apart lines are interspaced between said test pattern of parallel spaced apart lines formed in said first layer.

12. The process of claim 8 wherein said step of forming latent images of parallel spaced apart lines in said photoresist layer further comprises directing a first source of radiation onto said photoresist layer through a reticle patterned to provide a radiation image of said parallel spaced apart lines on said photoresist layer.

13. The process of claim 12 wherein said step of measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry further comprises directing a second source of radiation toward said latent images of lines in said photoresist layer and toward said test pattern of parallel spaced apart lines in said first layer.

14. The process of claim 12 wherein said first source of radiation used to form said latent images in aid photoresist layer comprises ultraviolet light.

15. The process of claim 12 wherein said second source of radiation used in said scatterometry to determine said alignment comprises visible light.

16. The process of claim 12 wherein said second source of radiation used in said scatterometry to determine said alignment comprises a radiation source selected from the group consisting of an electron beam, an ion beam, and a laser beam.

17. The process of claim 8 including the further step of forming a layer of metal interconnects over said first layer on said integrated circuit structure at least in fields not used for said alignment.

18. A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern of parallel spaced apart metal lines in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images of parallel spaced apart lines in portions of said photoresist layer lying in said selected fields overlying said test pattern of parallel lines of said first layer, said parallel lines of said test pattern of said first layer generally parallel with said parallel lines of latent images in said photoresist layer;

d) measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry; and

e) forming a further layer of integrated circuit structure over said first layer on said integrated circuit structure in fields not used for said alignment.

19. The process of claim 18 wherein said step of forming a further layer of integrated circuit structure over said first layer further comprises forming a layer of metal interconnects over said first layer on said integrated circuit structure in fields not used for said alignment.